

ATAM Course - Technion (Spring semester, 2023) Cheat Sheet by Ran RH via cheatography.com/180203/cs/39733/

Introduction

x86-64

In 64 bit processor, address size is 64 bit

Sizes	
Byte	8 bits
Word	16 bits
Double Word (DWORD) a.k.a Long Word	32 bits
Quadruple Word (QWORD)	64 bits

Endianness (Order of storing values)

For the Value: 0x01234567

Big Endian	0x100	0x101 23	0x102	0x103	
Little Endian	0x100	0x101	0x102	0x103	

Big Endian: The most significant value in the sequence is stored first, at the lowest storage address.

Little Endian: The least significant value in the sequence is stored first, at the lowest storage address.

In x86-64, Little Endian is used.

Virtual Memory Layout

General Purpose Registers

63	31	15	87 ()
%rax	%eax	%ax Xah	%a1	Return value
Xrbx	%ebx	%bx \[%bh	%b1	Callee saved
%rcx	%ecx	%cx Lch	%c1	4th argument
%rdx	%edx	%dx%dh	%d1	3rd argument
Krsi	Xesi	Xsi	%sil	2nd argument
Xrdi	%edi	%di	%dil	1st argument
%rbp	%ebp	%bp	%bp1	Callee saved
%rsp	%esp	%sp	%spl	Stack pointer
%r8	%r8d	%r8w	%r8b	5th argument
Xr9	%r9d	%r9w	%r9b	6th argument
%r10	%r10d %	r10w	%r10b	Caller saved
%r11	%riid %	riiw	%r11b	Caller saved
%r12	%r12d %	r12w	%r12b	Callee saved
%r13	%r13d %	r13w	%r13b	Callee saved
%r14	%r14d %	r14w	%r14b	Callee saved
%r15	%r15d %	r15w	%r15b	Callee saved

Special Registers

RIP (Instr-	Pointer to the next instru-
uction Pointer)	ction to run
RFLAGS	Saves the current state of
	the processor.

Both registers are 64 bits registers.

Assembly File Structure

```
.global _start # entry point
.section .data
index: .int 1
.section .bss
.lcomm final, 4
.section .text
_start:
    movl (index), %eax
    addl $5, %eax
    movl %eax, (final)
```

The assembly file is **divided into sections** using "Section Directives".

Moreover, the file can contain Global and External declarations, Directives, Labels, Comments, and of course, the assembly Instructions.

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