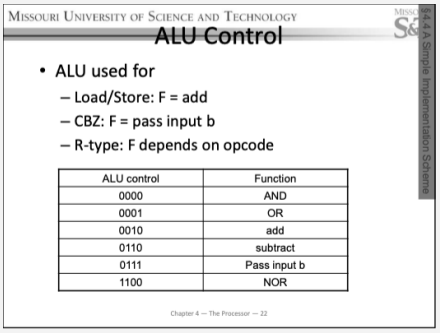
Cheatography

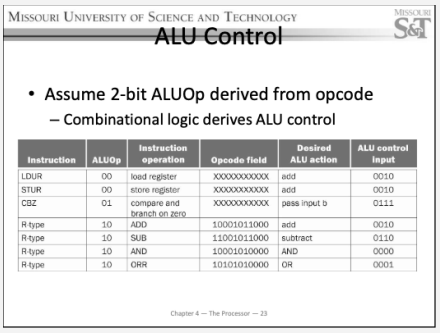
CpE 3110 Final Cheat Sheet

by datonecklund via cheatography.com/209963/cs/45231/

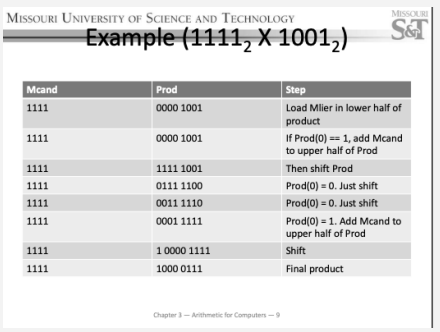
Alu Ctrl



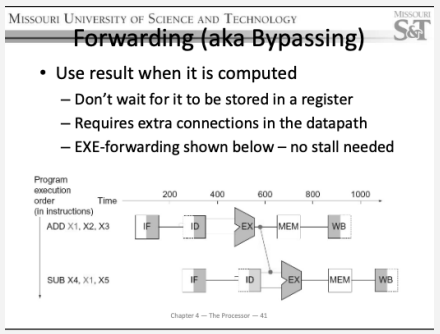
ALU Ctrl



upgraded adder table

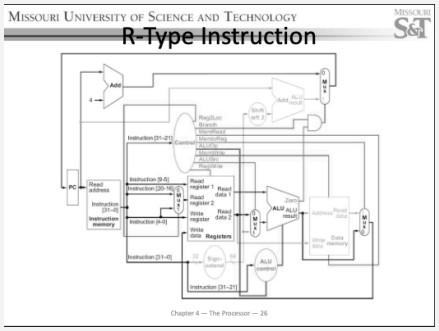


Forwarding

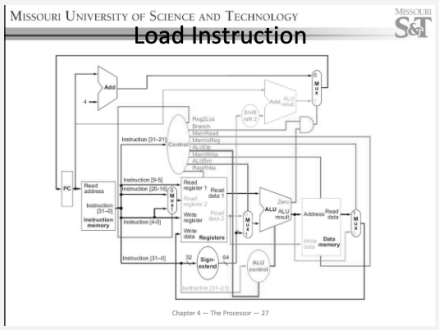


Forwarding(Men)

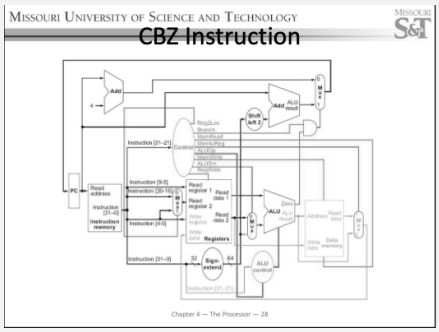
Control instructions



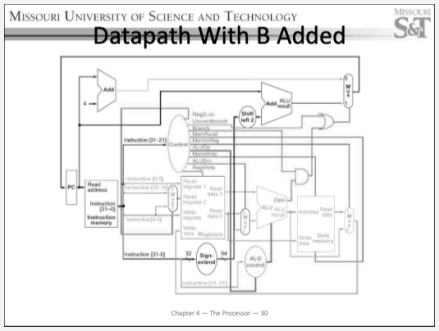
control instructions



control instructions



control instructions



Cashe Preformance

N-stage pipeline

P2 is a 7-stage pipelined processor with the clock cycle time of 200ps. If you are given a program with 1000 instructions without any pipeline hazards, calculate the execution times on P1 and P2

> P_2=(7*200ps)+(200ps*999 inits)

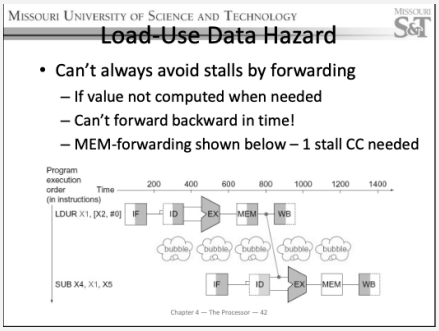
Hazards

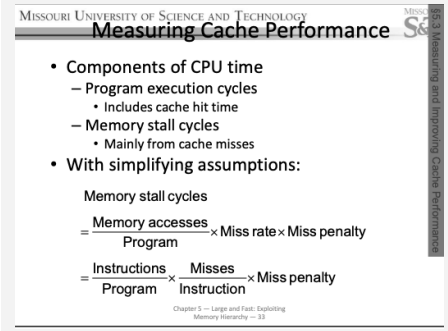
Structure Hazards	A required resource is busy
Data Hazards	Need to wait for previous instruction to complete its data read/write
Control Hazard	Deciding on control action depends on previous instruction

Pipeline stages

Five stages:

1. IF: Instruction fetch from memory
2. ID: Instruction decode & register read
3. EX: Execute operation or calculate address
4. MEM: Access memory operand
5. WB: Write result back to register





By **datonecklund**

cheatography.com/datonecklund/

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