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CSCI 2020 Computer Architecture

Basic binary math and logic Binary numbers operate in base 2, where the only digits are 0 and 1. They are fundamental in digital systems, logic design, and computing.

 Binary Arithmetic: Addition: Binary addition is similar to decimal addition, with the rules:
 Binary Subtraction: two's complement(invert bits add 1) of what is subtracting, add what is being taken from and discard carry

Logical Operations:

- AND (A * B): Outputs 1 only if both inputs are 1

- OR (A + B): Outputs 1 if at least one input is 1.
- XOR (A
 B): Outputs 1 if the inputs are different.
- NOT (¬A): Inverts the input.
 NAND (¬ (A * B)): Outputs 1 unless both inputs are 1.
- NOR (¬ (A + B)): Outputs 1 only if both inputs are 0.
- XNOR (¬ (A ⊕ B)): Outputs 1
 if the inputs are the same.
 Implication (A → B): Outputs 1

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unless A = 1 and B = 0.

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- Equivalence (A \leftrightarrow B): Outputs 1 if A and B are equal. Equivalent to XNOR. Total bit Combinations = 2ⁿ **Dec** \rightarrow **Hex** | Divide by 16, use remainders as hex digits. | 156 (dec) | 9C (hex) Hex → Dec | Multiply digits by 16ⁿ, sum the results. | 1A3 (hex) | 419 (dec) **Bin** \rightarrow **Dec** | Multiply bits by 2^n, sum the results. | 1101 (bin) | 13 (dec) Dec \rightarrow Oct | Divide by 8, use remainders as octal digits. | 125 (dec) | 175 (oct) **Bin** \rightarrow **Oct** | Group binary into 3 bits, convert each group to octal. | 110101 (bin) | 65 (oct) Sign Representation MSB(the front of bit): 0 (positive), 1 (negative) Negative: Invert and add 1 | | Arithmetic | Complex | Simplified (no separate subtraction) | | Range (4-bit) | (signed Magnitude((-7)) to (+7)(two's complement) (-8) to (+7 \) |

Combinational Logic

Combinational logic Definition

 Combinational Circuit: Output depends only on current inputs; no memory.
 Sequential Circuit: Output

depends on current inputs and past states (memory)

Key Differences

| Sequential Circuit |

-----|

| Output Dependency | Current inputs only | Current inputs + past states | | Memory | No memory | Has memory (e.g., flip-flops) | | Feedback | No feedback loop | Includes feedback loop | | Clock Signal | Not required | Requires a clock signal | | Time Dependency | Outputs appear immediately | Outputs depend on clock cycles | Examples

- Combinational Circuit:

Combinational Logic (cont)

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- Half Adder: Adds two inputs,
outputs Sum = (A XOR B),
Carry = \( A AND B ).
- Sequential Circuit:
- D Flip-Flop: Stores 1 bit of
data; updates on clock edge.
Applications
- Combinational Circuits:
- Adders, multiplexers,
encoders, decoders.
- Sequential Circuits:
- Counters, shift registers,
memory units.
Summary
- Combinational Circuits:
- Simple, stateless, used for
logical operations.
- Sequential Circuits:
- Complex, state-based, used
for time-sensitive or memory-
based tasks.
For AND(also minterm) gates
- Identity: AND-ing anything with
1 keeps it the same.
- Null: AND-ing anything with 0
makes it 0.
- Commutative: Changing the
order of inputs doesn't matter.
- Associative: Grouping inputs in
any way doesn't matter.
-Minterm = A \cdot B \cdot C \cdot D
```

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Combinational Logic (cont)

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- sum of products: Y=(A·B⁻·C·D)- $+(A^{-}\cdot B \cdot C \cdot D^{-})+(A \cdot B \cdot C^{-} \cdot D^{-})$ For OR(maxterm) gate - Identity: (A + 0 = A)- Null: \(A + 1 = 1 \) - Commutative: \(A + B = B + A - Associative: \(A + (B + C) = (A + B) + C \) - Idempotent: (A + A = A)- Distributive: - Over AND: \(A + (B AND C) = (A + B) AND (A + C) \) - Over OR: (A + (B + C) = (A + B) + C) -- Maxterm = (A^+B+C^+D) - Product of sums: Y=(A⁺+B+C--+D)·(A+B-+C+D-)·(A-+B-+-C⁺D) Prority Encoder Definition: A Priority Encoder is a combinational circuit that encodes the position of the highest-priority active input into a binary output. ently. Key Features: - Inputs: \(2^n \) input lines; only one active at a time is expected. - Outputs: \(n \) output lines representing the binary code of

Combinational Logic (cont) Combinational Logic (cont) - Priority: Higher-order inputs Delays occur when a circuit have precedence over lower-element transitions from 0 (low) order inputs. to 1 (high) due to physical and - Enable Output: Indicates if any electrical factors. input is active (optional). Key Causes of Delay Logic Expressions (4-to-2 1. Propagation Delay: Priority Encoder): - Time taken for a signal to - Y_1 = D_3 + D_2 propagate through a circuit - Y_0 = D_3 +{D_2}⁻ * D_1 element. - Enable Output (E = D_3 + D_2 - Affects overall circuit speed. + D_1 + D_0 2. Gate Capacitance: Applications: - Time required to charge or 1. Interrupt Handling: Assigns discharge the transistor's gate priority to multiple interrupt capacitance. signals in processors. 3. Load Capacitance: 2. Data Compression: Encodes - Higher load capacitance slows multiple inputs into fewer bits. the charging/discharging 3. Memory Decoding: Selects process. the highest-priority address or 4. Resistance of Interconnects: resource - Higher resistance in wires Advantages: increases \(RC \) delay. - Handles multiple inputs with 5. Signal Rise Time: priority logic. - Time taken for the signal to - Compresses input size efficirise from 10% to 90% of its final value. Limitations: 6. Threshold Voltage: - Requires additional handling if - Higher voltage thresholds multiple inputs have the same cause slower transitions. priority. 7. Noise and Signal Integrity: - Extra circuitry needed for "no - Crosstalk, interference, or active input" conditions. power fluctuations can distort Causes of Delay in Circuit State signals. Change (Low to High) 8. Power Supply Voltage: Definition:

- Lower voltages reduce drive strength, increasing delay. 9. Temperature Effects:

Combinational Logic (cont)

- High temperatures slow down transistor switching.

10. Manufacturing Variations:

- Fabrication inconsistencies can result in slower components.

11. Clock Synchronization:

- Skew or jitter in clock signals causes timing delays in sequential circuits.

12. Parasitic Elements:

- Unintended resistance, capacitance, or inductance contributes to delay.

Summary:

Delays result from intrinsic (e.g., propagation, capacitance) and external factors (e.g., noise, temperature). Optimizing design and materials can mitigate these delays.

Combinational Logic

Combinational logic Definition

- Combinational Circuit: Output depends only on current inputs; no memory.

- Sequential Circuit: Output depends on current inputs and past states (memory)

Key Differences

| Feature | Combinational Circuit | Sequential Circuit |

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the highest-priority input.

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Combinational Logic (cont)

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Combinational Logic (cont)

Combinational Logic (cont)

Combinational Logic (cont)

	- Combinational Circuits:	Maxterm = (A ⁺ +B+C ⁺ D)	3. Memory Decoding: Selects
	- Simple, stateless, used for	- Product of sums: Y=(A ⁺ +B+C-	the highest-priority address or
	logical operations.	-+D)·(A+B ⁺ +C+D ⁻)·(A ⁺ B ⁺ +-	resource.
Output Dependency Current	- Sequential Circuits:	C ⁻ +D)	Advantages:
inputs only Current inputs +	- Complex, state-based, used	Prority Encoder	- Handles multiple inputs with
past states	for time-sensitive or memory-	Definition:	priority logic.
Memory No memory Has	based tasks.	A Priority Encoder is a combin-	- Compresses input size effici-
memory (e.g., flip-flops)	For AND(also minterm) gates	ational circuit that encodes the	ently.
Feedback No feedback loop	- Identity: AND-ing anything with	position of the highest-priority	Limitations:
Includes feedback loop	1 keeps it the same.	active input into a binary output.	- Requires additional handling if
Clock Signal Not required	- Null: AND-ing anything with 0	Key Features:	multiple inputs have the same
Requires a clock signal	makes it 0.	- Inputs: \(2^n \) input lines; only	priority.
Time Dependency Outputs	- Commutative: Changing the	one active at a time is expected.	- Extra circuitry needed for "no
appear immediately Outputs	order of inputs doesn't matter.	- Outputs: \(n \) output lines	active input" conditions.
depend on clock cycles	- Associative: Grouping inputs in	representing the binary code of	Causes of Delay in Circuit State
Examples	any way doesn't matter.	the highest-priority input.	Change (Low to High)
- Combinational Circuit:	-Minterm = $A \cdot B^- \cdot C \cdot D^-$	- Priority: Higher-order inputs	Definition:
- Half Adder: Adds two inputs,	- sum of products: Y=(A·B ⁻ ·C-	have precedence over lower	Delays occur when a circuit
outputs Sum = \(A XOR B),	·D)+(A ⁻ ·B·C·D ⁻)+(A·B·C ⁻ ·D ⁻)	order inputs.	element transitions from 0 (low)
Carry = \(A AND B).	For OR(maxterm) gate	- Enable Output: Indicates if any	to 1 (high) due to physical and
- Sequential Circuit:	- Identity: \(A + 0 = A \)	input is active (optional).	electrical factors.
- D Flip-Flop: Stores 1 bit of	- Null: \(A + 1 = 1 \)	Logic Expressions (4-to-2	Key Causes of Delay
data; updates on clock edge.	- Commutative: \(A + B = B + A	Priority Encoder):	1. Propagation Delay:
Applications	\)	- Y_1 = D_3 + D_2	- Time taken for a signal to
- Combinational Circuits:	- Associative : \(A + (B + C) = (A	- Y_0 = D_3 +{D_2} ⁻ * D_1	propagate through a circuit
- Adders, multiplexers, encoders,	+ B) + C \)	- Enable Output (E = D_3 + D_2	element.
decoders.	- Idempotent: $(A + A = A)$	+ D_1 + D_0	- Affects overall circuit speed.
- Sequential Circuits:	- Distributive:	Applications:	2. Gate Capacitance:
- Counters, shift registers,	- Over AND: \(A + (B AND C) =	1. Interrupt Handling: Assigns	- Time required to charge or
memory units.	(A + B) AND (A + C) \)	priority to multiple interrupt	discharge the transistor's gate
Summary	- Over OR: (A + (B + C) = (A +	signals in processors.	capacitance.
	B) + C)	2. Data Compression: Encodes	3. Load Capacitance:
	. ,	multiple inputs into fewer bits.	- Higher load capacitance slows

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process.

the charging/discharging

4. Resistance of Interconnects:

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Combinational Logic (cont)

- Higher resistance in wires

increases \(RC \) delay.

5. Signal Rise Time:

- Time taken for the signal to rise from 10% to 90% of its final value.

6. Threshold Voltage:

- Higher voltage thresholds cause slower transitions.

7. Noise and Signal Integrity:

- Crosstalk, interference, or power fluctuations can distort signals.

8. Power Supply Voltage:

- Lower voltages reduce drive strength, increasing delay.

9. Temperature Effects:

- High temperatures slow down transistor switching.

10. Manufacturing Variations:

- Fabrication inconsistencies can result in slower components.

11. Clock Synchronization:

- Skew or jitter in clock signals causes timing delays in sequential circuits.

12. Parasitic Elements:

- Unintended resistance, capacitance, or inductance contributes to delay.

Summary:

Combinational Logic (cont)

Delays result from intrinsic (e.g., propagation, capacitance) and external factors (e.g., noise, temperature). Optimizing design and materials can mitigate these delays.

Sequential Logic

State Table for A, B, Clock and XOR gate what is Q?

To determine the contents of the output register Q, we'll use a **state table** that describes the relationship between the inputs A, B, the clock, and the XNOR gate, along with the resulting Q. **XNOR Gate Logic**

- The output of an XNOR gate is A↔B (logical equivalence):

 $- A \oplus B = 0: (A \oplus B)^{-} = 1$ (when A = B)

- $A \oplus B = 1 (A \oplus B)^{-} = 0$: (when $A \neq B$)

The output Q of the register will update on every clock edge based on the XNOR output. State Table

Assume:

Inputs A and B are parallel inputs (change at each clock cycle).
Register Q is updated at every

positive clock edge with the XNOR output.

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